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SATELLITE-ON-A-CHIP FEASIBILITY FOR DISTRIBUTED SPACE MISSIONS

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ABSTRACT
A new dimension of space mission architecture design is emerging where hundreds to thousands of very small satellites will collectively perform missions in a distributed fashion. To support this architecture, high volume production of femto-scale satellites at low cost is required. This paper reports on the assessment of using SpaceChip, which is a monolithic "satellite-on-a-chip" based on complementary metal-on-silicon (CMOS) technology, for limited distributed space missions.

INTRODUCTION
Novel techniques are required for very small satellite (VSS) designs to support the surging demand for missions based on new distributed satellite system (DSS) architectures. Due to the success of early DSSs such as GPS and IRIDIUM, new Earth-orbiting and interplanetary mission concepts are emerging that require hundreds to thousands of VSSs, analogous to wireless sensor networks in space. In order to support these large numbers with unavoidable budget and launch vehicle constraints, a flexible and mass-producible VSS bus design is needed. To support the claim for such a bus, an overview of distributed space missions (DSMs) is presented first, clarifying common and often misused terms such as *swarms*, *clusters*, and *formation flying.*

This paper reports on the assessment of using SpaceChip, which is a monolithic "satellite-on-a-chip" based on complementary metal-on-silicon (CMOS) technology, for limited distributed space missions. SpaceChip is part of a larger research effort to optimise VSS design for a selection of DSMs where real-time, simultaneous, and distributed sensing is required [1].

DISTRIBUTED SPACE MISSIONS REVIEW
The interchangeable terms, *distributed satellite system* and *distributed space system*, now evokes the promise of realising satellite missions that have not been previously possible, although the DSS concept has existed since the first satellite constellation. Burns defines a DSS as "an end-to-end system including two or more space vehicles and a cooperative infrastructure for science measurement, data acquisition, processing, analysis and distribution" [2]. Jilla offers a more simple definition, where a DSS is "a system of multiple satellites designed to work in a coordinated fashion to perform a mission" [3].

However, Shaw offers the most complete definition [4]. In summary, he notes that there are really two accepted definitions for a DSS. The first definition, which is defined in this paper as Type I hereafter, describes missions where multiple satellites are sparsely distributed using traditional constellation designs in order to meet various mission requirements. Type I scenarios do not typically require precision orientation between spacecraft and may not employ any propulsive stationkeeping. Traditionally, multiple satellites are connected via ground systems. More recently, crosslinks have enabled a higher degree of autonomy and interconnectivity. As will be presented in the upcoming examples, just about any satellite system employing a constellation of two or more satellites qualifies as a Type I DSS.

Shaw goes on to discuss the Type II scenario, which introduces the concept of a local "cluster," where satellites are more closely spaced in the same orbit and are trained together on a common target. Optionally, this cluster of satellites may have a more complex configuration, namely a "formation." Formation flying requires that satellites in a cluster maintain precise spacing and orientation relative to each other, with the level of precision based on mission requirements. This directly implies that the spacecraft must have precision location knowledge of each other and a propulsion system to maintain the formation, as a formation cannot naturally exist in orbit. The basic idea behind formation

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flying is to synthesise an aperture, antenna, or some other sensor suite for the purpose of achieving performance levels that cannot be achieved by the largest satellite today performing a similar mission. To date, most aspects of this concept have been widely studied, but the first implementation has yet to be realised, with the exception of a few crude experiments.

Figure 1 illustrates the basic breakdown of DSSs as commonly found in the literature. These relationships will be important to remember while reviewing the related missions and systems. The focus of this research is on space sensor networks implemented as Type I with crosslinks.

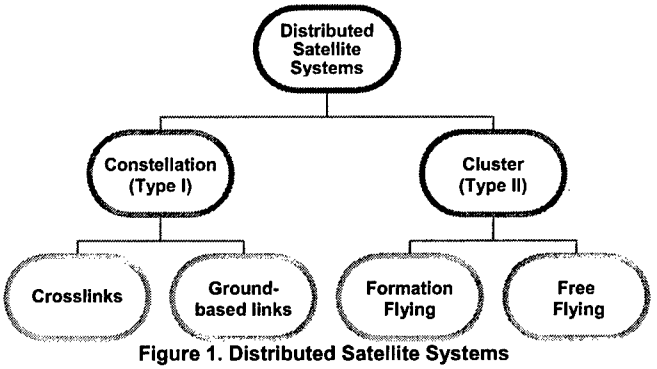

Figure 1. Distributed Satellite Systems

Garrison summarises the first, largest, and best example to date of a Type I DSS: the IRIDIUM global communications system launched in 1997 [5]. IRIDIUM is a constellation of 66 satellites, each weighing 689 kg (considered a medium or large satellite), which provides global telecommunications services with very low latency to users with compact handsets. The system has some autonomy with very low communication latency due to RF crosslinks.

Peters points out that IRIDIUM is the only commercial system to date that employs RF crosslinks [6]. Although everyone realizes the phenomenal advantages of crosslinks, their additional cost and complexity have won out and prevented any new systems from being fielded. As mentioned previously, the MILSTAR system is the only military system currently using RF crosslinks. The next generation of U.S. military satellites will employ optical (laser) crosslinks and downlinks, providing an order of magnitude increase in capability [7].

Users worldwide currently leverage the use of the U.S. Air Force Global Positioning System (GPS) constellation [8]. The constellation is now composed of 24 satellites in semi-synchronous orbits, placed evenly in six planes designed to provide position and timing information to users on land, sea, and in the air. Space systems have demonstrated the use of GPS for orbit determination.

The Russians operate a similar system called GLONASS that utilizes 12 to 14 satellites in two planes [9]. The European Union recently funded and launched a technology pathfinder mission to explore the feasibility of fielding their own system, named Galileo [10]. All three navigation systems discussed are clearly a Type I DSS that do not employ crosslinks.

Commercial imagery applications are also widespread where satellites take visible and IR images of specific regions of interest in the world. Commercial imagery is used for mapping requirements, agricultural data, disaster monitoring, and other generic requirements. Systems such as QuickBird, OrbView, IKONOS, SPOT, and Landsat offer resolutions as good as 0.6 meters and are all classified as medium to large satellites. However, none of these systems can be classified as a DSS, as they are all single-satellite systems, although some recent consolidation in the industry has put forth the claim of new imaging constellation.

Small satellites have recently entered the earth imaging market. A recently completed Disaster Monitoring Constellation (DMC) of five 166 kg earth-imaging mini-satellites offers an unprecedented revisit time of 24 hours, versus days or weeks from other commercially available imaging systems [11]. The DMC is considered the first Type I Earth Imaging DSS.

PROPOSED DISTRIBUTED SPACE MISSIONS

There has been a recent literary explosion, in terms of DSS related topics in the past 10 years. In publications of the American Institute of Aeronautics and Astronautics (AIAA) alone, the terms "distributed satellite systems," "satellite formation flying," and "satellite cluster" have become very hot topics over the past ten years as highlighted in Table 1. The mention of "satellite cluster" in literature dating 1995 and earlier, denoted with an asterisk, is exclusively on the topic of placing satellites at very close distances in the GEO belt to address the crowding issue there.

Table 1. DSS Terms in the Literature

Year	"Distributed Satellite Systems"	"Satellite Formation Flying"	"Satellite Cluster"
<1991	0	0	19*
1991-1995	0	0	9*
1996-2000	5	16	23
2001-2006	33	82	82
Total	**10**	**98**	**105**

The majority of new DSS concepts are of the remote sensing, scientific, and interplanetary exploration types. For completeness, suggested reasons for non-proliferation of new DSS systems in the communication and navigation areas are presented first.

With the IRIDIUM, Globalstar, and ORBCOMM constellations in their current state of poor financial health, Ashford notes that current realities have shattered all the previous predictions of a rapidly increasing demand for LEO-based comm DSMs [12].

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Norris has proposed that clusters of small satellites operating in LEO will eventually be used to "virtually" replace larger monolithic telecommunication satellites [13]. There may be a demand for this someday as the GEO belt fills up, especially over the most populated areas of the earth. Another variant of this idea, put forth by Edery-Guirardo, is to augment larger satellite missions with a constellation of smaller communication relay satellites [14]. For the time being, large satellites in GEO appear to be the mainstay of high-bandwidth global communications.

One notable large-scale communication DSM that never left the drawing board was the Teledesic system. With conceptual designs proposing up to 840 satellites, Teledesic was to provide the first global "internet in the sky" for the entire globe.

The GPS, GLONASS, and up and coming Galileo mission have already been categorised as Type I DSSs. However, nowhere in the literature has anyone proposed a Type II mission or a larger-scale Type I mission. The logical explanation for this is that the current navigation systems have known vulnerabilities to jamming [15]. For the GPS system in particular, next generation systems will mitigate this vulnerability with the combination of higher power RF signals with other anti-jam technologies, causing the mass to rise from the current 1,000 kg to an estimated 1,500 kg [16]. The jamming environment will only get worse, requiring increased RF power from space. This trend does not facilitate the use of microsatellites or smaller, formation flying or not.

There are numerous envisioned remote sensing DSSs, however none of them have gone beyond the concept phase. The following are examples where large numbers of very small satellites are required:

- Volcano, fire, or earthquake warning and detection
- Treaty monitoring sentinels
- Distress beacon monitoring on a global basis
- Military application for space control [17]

More advanced applications which require adaptation and reconfiguration in the node for various wireless parameters are as follows:

- Beam forming to remotely sense a particular location
- To minimise power expenditure by optimising the RF link budget, e.g. in the event of interference or particularly good transmission conditions
- Constellations based on highly robust low cost VSSs, applying lessons learnt from the DMC but for a wider range of applications, and at lower cost.
- In particular imaging with frequent temporal repeats and high spatial resolution
- A constellation where users can access the services of the entire group, but at the low cost of a node
- Signal intelligence e.g. for tactical / military apps

Das was the first to propose space based radar could be more effectively employed with formation flying clusters [18]. Similarly, multistatic radar may also be possible. Co-orbiting assistants/inspectors of larger mother ships such as large satellites, the space shuttle or the international space station could be considered Type II if used in clusters as presented by Macke [19]. Zencik proposes the use of GPS in cluster management [20].

Science and exploration missions are also a very promising area for very small satellites, with many proposals put forth employing a formation flying or swarm concept. These Type II concepts will be discussed in the next section. Below is a list of proposed missions that require a Type I configuration:

- A proposed magnetospheric constellation mission that may reveal how the magnetotail behaves in response to solar wind variations among other fundamental scientific data [21]
- NASA's ultimate goal for widespread interplanetary exploration is based on the satellite-on-a-chip [22]
- Monitoring and warning of large area space phenomena, notably Space Weather
- Monitoring wide area highly time dependant phenomena, e.g. Aurora
- Detailed characterisation of environments to support exploration e.g. MARS atmosphere, Asteroid belt, other planetary atmospheres, etc.
- Upper atmosphere monitoring, e.g. CO_2 levels in the altitude range 60-250km
- Lower atmosphere sounding, where rockets launched from Earth are too short duration and costly, and conventional large satellites cannot cost-effectively operate low enough without large propellant expenditures - piconodes with low enough ballistic coefficients, could be launched and allowed to drift down through the atmosphere over short periods - effectively disposable satellites

For more advanced missions, reconfigurability of the nodes would be required:

- Measuring ion or electron scale space weather events and effects within the magnetosphere (10's of meters to km's)
- To compensate for interference from other sources such as radiation (lightning in storms, trapped radiation e.g. South Atlantic Anomaly, stray electromagnetic fields) for example by frequency hopping

There are only two serious Type II science and exploration DSMs that are being considered. The highest profile mission is NASA's Terrestrial Planet Finder (TPF) mission [23]. TPF will rely on a formation flying cluster at the one of the Sun-Earth libration points to synthesise a very large aperture to see farther in the universe with unprecedented resolution. A simpler Type II mission is to measure variations in magnetic fields

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around a spacecraft, perform visual inspection of a spacecraft exterior for signs of damage, rapidly map an asteroid, or perform in-flight calibration of a communications beam pattern using deployable inspector spacecraft [19].

HISTORY OF VERY SMALL SATELLITES

Since the dawn of the space age in 1957, increasing mission requirements have driven up satellite mass from Sputnik's 84 kg to over 5,000 kg for some systems today. Consequently, cost, complexity, program timelines, and management overhead have grown considerably. Reversing this trend, a fast-growing small satellite industry, launched by academia, has enabled increasingly capable and cost-effective space missions based on sub-500 kg satellites by embracing smartly reduced requirements and commercial technology.

In order to appreciate the capabilities of small satellites, the community has developed a set of mass classifications as shown in Table 2. The preponderance of missions to date has been in the minisatellite and microsatellite ranges. A mass histogram is shown in Figure 2 [24].

Table 2. Small Satellite Categories

Minisatellite	100 - 500 kg
Microsatellite	10 - 100 kg
Nanosatellite	1 - 10 kg
Picosatellite	100 g - 1 kg
Femtosatellite	1 - 100 g

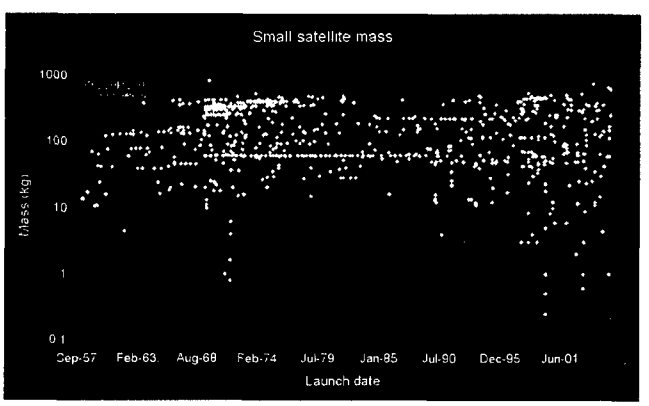

Figure 2. Small Satellite Mass Histogram

Although micro- and minisatellites have had the most activity, this research is scoped at looking at the downward trend from nanosatellites, to picosatellites, to femtosatellites. A histogram over the past fifteen years of sub-10 kg missions is given in Figure 3 [24]. The next section discusses proposed requirements for spacecraft designed for DSSs.

As one can see, there over a dozen nanosatellites have flown over the past ten years. The most notable nanosatellite that has flown to date is SNAP-1, which was the first nanosatellite with full attitude and orbit determination and control capabilities [25].

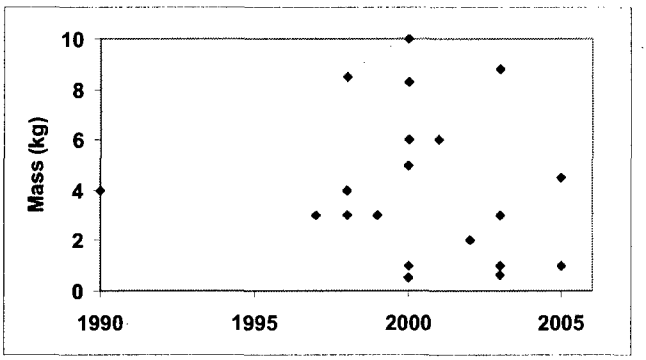

Figure 3. Very Small Satellite Mass Histogram

Two notable nanosatellites are in development at this time. The first is the recently renamed MicroLink-1, which is very focused on developing multifunctional modules to enable mass production of nanosatellites through the CANEUS NPS consortium [26][27]. The other is the recently completed ESA study "Nanosatellite Beacons for Space Weather Monitoring" [28].

Fourteen picosatellites have flown in the past ten years. Of those, eight were "CubeSats," which is a university student satellite standard defined by Stanford and Cal Poly. The first picosatellite mission flew in 2000, which was dubbed the Orbiting Picosatellite Activated Launcher (OPAL) [29]. Six custom picosatellites were launched, but only two worked for a short duration. In 2003, the Eurockot launch deployed five CubeSats, but only three were declared successful. Recently, in 2005, the SSETI Express deployed three CubeSats, with two being successful. Overall, picosatellites have only had a 50% success rate, with most of the failures attributed to poor electrical power subsystem design.

One picosatellite in development at SSC is Palmsat [30][31]. Unlike the CubeSat standard, Palmsat offers more capability with deployable solar arrays.

To date, no femtosatellite has ever been launched into space. Cyrospace claims to have designed a femtosatellite, but attempts to correspond with the company or find anything published in the literature have turned up negative results [32]. Helvajian and Janson have orchestrated a femtosatellite design based on MEMS and micromachining of glass [33]. Much more of their work will be presented later, but they are mainly focused on innovative structures and propulsion.

HISTORY OF SATELLITE ON A CHIP

This section gives a history of all mentions of the term "satellite-on-a-chip" or "spacecraft-on-a-chip" in the literature. It is presented chronologically in time by paragraph. Within each paragraph, the complete history of the original finding is outlined.

The first mention of satellite-on-a-chip comes from an interview with A. Joshi, founder of Discovery Semiconductor, New Jersey in 1994 [34]. In the

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interview, he is quoted as saying "We want to integrate more functions of a satellite on a semiconductor chip to shrink the payload in weight...this project will tell us if we can integrate more on the same chip down the road, and be able to get a whole instrument on a chip." The interview concludes with his stated goal of blending electronic, optics, and micro electrical mechanical system (MEMS) on a single chip. In 1998, we see another news interview with A. Joshi, proposing an Integrated Satellite (INT-SAT) [35]. The core of the design is several "wafer size chips" which eventually lead to a satellite mass "below 10 kg." Also, in 1998, he proposed a "monolithic infrared detector array" that supports the satellite-on-a-chip idea [36]. Later in 2000, A. Joshi secured a U.S. patent on the topic, with a "stacked array" of wafers at the core of the INT-SAT design [37]. Although a promising set of references, no other work has been published in scholarly journals.

The next thread of discussion was in 1995, buried in a 120-page final report for a military education course [38]. In the report, the president of AeroAstro was quoted as predicting that "a $100,000 satellite-on-a-chip could be available by the end of the decade and would cost less that $50 million to develop." This quote is replicated among a few other published interviews. His prediction was not realized, nor has AeroAstro published any significant progress on the idea.

NASA was the next organization to jump on the bandwagon in 1997 [22]. They launched the New Millennium program, where "The objective is to leap-frog currently planned technology developments to fulfil the long-term vision of a spacecraft on a chip, accomplishing all electronic, power control, computational, and communications functions on small integrated chips." The New Millennium program supports new deep space missions. In 1998, they launched a related education initiative—the Deep Space Systems Technology Program (X-2000) that encouraged students to learn about spacecraft avionics and presented that in the future spacecraft-on-a-chip would be a reality [39]. From this time, NASA has widely been involved with and supported countless spacecraft miniaturization efforts.

The next rash of interest starts in 1999. Janson of The Aerospace Corporation, California, is quoted with "The goal is to one day build a satellite on a chip [40]." In a related article, Panetta, manager at the time of NASA's nanosatellite program, was quoted with "If you really want to think far reaching, there's the possibility of a femtosatellite, essentially a solid-state satellite on a chip, weighing 100 grams or less [41]." This is the first mention of the term "femtosatellite" in the literature. The term is again mentioned in a related article in 2000 [42].

Starting in 2000, the Surrey Space Centre (SSC) is the next organization to start referencing the idea, focusing on the data processing a control element [43]. They launched a web page in 2002 on the idea, codenaming it "ChipSat [44]." Unfortunately, another unrelated mission called "CHIPSat" botched the term with their acronym that stands for Cosmic Hot Interstellar Plasma Spectrometer Satellite. In 2003, the Centre sponsored a master's thesis on integrating communication functionality into a small satellite system-on-a chip (SoC) on-board computer (OBC) [45]. The idea was again advertised on a new website later that year [46]. That same year in a presentation with their partner commercial company, Surrey Satellite Technology Ltd. (SSTL), their internal research and development portfolio suggested that they were working "towards satellite-on-a-chip [47]." In an aggressive move in 2005, they presented a basic outline and initial design of a satellite-on-a-chip [1]. There are only a handful of other related references that can be found in the literature, suggesting this area is ripe for novel work.

EMERGING SATELLITE-ON-A-CHIP TECHNOLOGIES

At the beginning of the satellite-on-a-chip work, the monolithic approach was viewed as truly encompassing the spirit of the idea. As will be discussed in the design concept in the next chapter, the monolithic approach does have limits. One of the limits is that a complete design cannot exceed the reticle, which is limited by the size of the mask set, which is used in the photolithography process to fabricate devices. In general, this limitation limits the maximum die size to approximately 360 mm^2 for modern processes, although it generally grows over time.

To overcome this size limit, in the 1990s a technique called wafer-scale integration (WSI) was proposed and developed [48]. WSI allows for multiple reticle-sized designs to be co-located on the same wafer, and then connected together using various interconnection techniques, allowing for a final product that in theory could be as large as the entire wafer, which can be from 100-300 mm in diameter. Unfortunately, the inherent defects in the semiconductor manufacturing process frustrated this idea and therefore never really saw widespread adoption [49].

MCM technology has quickly replaced the void that WSI was supposed to fill far large-scale system-on-a-chip concepts [49]. An emerging variant of MCM technology is a three-dimensional approach [50]. Although it offers higher density packaging, it is still more expensive than and not as accessible as traditional PCBs. Advancements in individual IC packaging are keeping PCBs a very affordable option. However, for high-density system-in-package efforts, MCM technology is becoming the preferred approach [51].

As will be discussed in the design, a simple CMOS imager was selected as the payload for the satellite-on-a-chip feasibility study. Yadid-Pecht and Etienne-Cummings recently published in 2004 the definitive work for CMOS imaging technology [52]. This text clearly outlines how to build a CMOS imager and gives results

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from many successful designs. However, it is highlighted in the Preface that the technology will should soon be incorporated in systems-on-a-chip.

We can confidently assume at this point that challenges in the power distribution, regulation, and control design can be met with basic wiring, switching, and regulation circuitry that are routinely implemented in CMOS [53]. The real challenge is integrated solar cells on CMOS. In general, solar cells are predominantly fabricated with modified silicon (Si) and Gallium Arsenide (GaAs) technologies, using distinctly different processes than ones used for CMOS digital electronics.

Integrating solar power with digital circuitry has not been of interest until recently, with efforts like "Smart Dust," however, most of these concepts rely on MCM-type integration [54]. One very promising example demonstrates monolithically integrated solar-cells, CMOS transistors, and a basic MEMS structure built on a highly-modified silicon-on-insulator (SOI) process [55]. Although SOI is growing in popularity, it is not yet a widely available commercial technology.

Truly monolithic self-powered devices on bulk CMOS have been designed, built, and successfully tested. Three good examples are a wireless sensor network node [56], an implantable device to restore loss of human sight [57], and other basic research [58]. Unfortunately, none of these publications addressed the issue of efficiency specifically. The other authors were unreachable, but in private correspondence with Blaauw, it was revealed that their efficiency was less than 1%.

To further understand the issue, Castañer, an expert in solar cell design, was contacted via e-mail for assistance [59]. His overall recommendation was as follows: "People tend to process separately CMOS and PV modules and try to package them using high density packaging or hybrid packaging and then can get the most of the two separate technologies."

He offered a more detailed explanation: "In my view all CMOS technology is not very careful with the value of the carrier lifetimes in the processed devices as CMOS transistors are not sensitive to those parameters to a large extent. However solar cells are, so using the same CMOS process to build solar cells will end up with low efficiency. Moreover in order to build series arrays (which you need in order to raise the output voltage to meet the load requirements), you are very limited as you will be using the well of the p-MOS transistors to build the base of the solar cells. This ends up with very shallow devices, and as silicon is an indirect gap material, the efficiency is very sensitive to the thickness of the effective base layer. In addition to that I don't know if the CMOS people will be happy having a lot of carriers in the bulk not collected by the solar cells which are at the top." Obviously, commercial CMOS presents a challenge here.

Instead of implementing a full-featured CPU on the satellite, we will utilize a reduced instruction set (RISC) design that takes up less space and power. In academia, some introductory thought has been given to miniaturizing flight computer components to a single chip [60]. There is also some complementary industry interest in the topic [61]. These efforts all stem from a growing trend in developing system-on-a-chip for various applications, including space.

Chien has written the definitive work for single-chip digital radio technology [62]. The text gives a very good overview of digital radio basics and a supporting overview of spread-spectrum communications. Then the text reviews the design details for the RF and radio portions of a communication device. The text concludes with three very helpful chapters on digital RF design, digital radio design, and example single-chip digital radio implementations. It even suggests that single-chip radio designs should be monolithically integrated with other systems.

Despite the solar cell difficulties, the communication subsystem will turn out to be the chief limiting factor that governs satellite-on-a-chip applicability. Even if sufficient solar power can be generated to produce the corresponding downstream RF power, the limiting factor is the effectiveness of integrated antennas on CMOS [63]. Currently the maximum range is only a few meters.

EMERGING VSS FABRICATION TECHNOLOGIES

Since 1998, Helvajian and Janson have pioneered the idea of microengineering of aerospace systems [64]. The next year, Helvajian published the first text on the subject [65]. Helvajian has worked closely with Janson, both working for the Aerospace Corporation, El Segundo, CA, who have published several recent works on various VSS concepts, usually based on MEMS and/or micromachining [66]. One of the earliest approaches was an "all silicon" approach, where the satellite is constructed with miniature components [67]. Janson only touches on leveraging CMOS technology [68] while continuing to inform the space community of the upcoming emergence of technologies specifically target at developing VSSs [69]. A further refinement of the idea uses glass and ceramic materials to make specific parts of the satellite, such as the structure and propulsion subsystems [70].

Around the time Helvajian and Janson introduced these ideas, Xuwen and later Shul, published similar concepts, but no follow-on effort has emerged [71][72]. During this same time, the concept of multifunctional structures and architectures are starting to emerge to support the idea of mass production of very low cost VSSs [73]. This thought fostered the "responsive space" movement [74], where satellite systems could be built and deployed very rapidly based on leveraging streamlined manufacturing processes and modular technologies [75].

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SATELLITE-ON-A-CHIP FEASIBILITY STUDY

SpaceChip is the "codename" for the first satellite-on-a-chip endeavour. Along with the literature review of satellite-on-a-chip presented in Chapter 2, this feasibility study is simply a "back of the envelope" design using Wertz and Larson's Space Mission Analysis and Design (SMAD) principles [76]. Most space systems engineering projects begin with a known mission to accomplish. In this case, the "mission" was to determine what the technical limitations of a satellite-on-a-chip would be.

A mission statement is composed of an objective, the users, and the operations concept. The primary SpaceChip mission objective is to demonstrate the feasibility of satellite-on-a-chip technology. The second objective is to take a low-resolution image of the earth in LEO and transmit it to a ground station.

The users of SpaceChip will initially be the author and the Surrey Space Centre. Once proven, the user base will grow based on the interest in using satellite-on-a-chip technology to enable envisioned and yet-to-be-discovered distributed mission concepts.

The initial operations concept will be to deploy a small number of SpaceChips from a host nano- or microsatellite in LEO. The mission objective is to be performed within a week of separation. This host satellite will serve as the communications relay to transmit SpaceChip data to the SSTL ground station.

Based on the mission statement developed in the previous section, a set of system requirements were derived. These system requirements will be used to focus the design of SpaceChip:

Top Level Requirements
- SpaceChip must be implemented on a commercial CMOS process, suitable for integration of digital, analogue, and RF components
- SpaceChip must meet all mission objectives and support the operations concept

Payload Requirements
- The payload will be a CMOS imager with 4,096 pixels in a 64x64 arrangement

Orbit Requirements
- SpaceChip will be designed to operate in LEO

Configuration and Structure Requirements
- SpaceChip will closely conform to the monolithic "satellite-on-a-chip" definition
- SpaceChip will not exceed the typical CMOS process reticle limit of 18 x 20 mm
- 10 g or less in mass
- Interface and ejection mechanism from host spacecraft or launcher

Electrical Power Subsystem Requirements
- The power source will be solar energy via integrated photovoltaic cells
- Investigate secondary power options for eclipse periods

Data Handling Requirements
- Minimal microcontroller to perform mission with possible non-volatile memory
- Radiation hardening by design to prevent latchup and minimize single event upset

Communication Requirements
- Digital transceiver in unlicensed 2.4 GHz Instrumentation, Scientific, Measurement band
- Each SpaceChip will have a unique identification number
- Investigate maximum range to determine communication architecture

Attitude Determination and Control Requirements
- No attitude determination requirement
- Investigate passive attitude control techniques for optimal solar power collection

Orbit Determination and Control Requirements, including Propulsion
- Investigate technologies

Thermal Control Requirements
- Passive control

SPACECHIP PAYLOAD SELECTION

Initially, a survey of potential payloads was performed to determine what payload could be integrated onto a CMOS die that could demonstrate a recognizable mission. MEMS payload options were primarily eliminated due to the fact that they could not be monolithically integrated in CMOS. Secondary reasons were based on size, mass, or power requirements that seemed impossible to meet. The search quickly revealed only one suitable payload—a digital imager.

Charge coupled devices (CCD) have been the mainstay of digital imaging. CCDs, however, have some major disadvantages concerning our application. They are built using non-mainstream semiconductor fabrication techniques, have a relatively high power requirement, and cannot be integrated with support circuitry monolithically with standard complementary metal-on-silicon (CMOS) processes. However, in the last decade, monolithic digital imagers built in CMOS have become a promising technology and may eventually replace CCD technology. Not only is it convenient for monolithic CMOS integration, it is inherently low power and more sensitive, although the image quality is not as good [77].

The definitive text on CMOS imagers gives an overview of silicon-based phototransduction, with a complete comparison of CCD and CMOS technologies [52].

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CMOS-based technology is thereafter referred to as an active pixel sensor (APS). A chapter on modelling and one on analysis follow, which lead into the most important chapter, APS design. The APS design chapter highlights a CMOS APS test chip fabricated in Hewlett-Packard (HP) 0.5 μm technology. The APS chip featured a very low power 64 x 64 pixel array. The technique presented in this chapter is easily repeatable and has obviously been demonstrated in CMOS. This design will be the baseline for the SpaceChip payload. The issue of a lens requirement has arisen, but a promising solution is an integrated diffraction lens recently demonstrated [78].

SPACECHIP CONFIGURATION AND STRUCTURE

Once the payload is defined, the most important thing to do first is to develop the spacecraft configuration. The "configuration" describes the physical relationship between the payload and subsystem components. Usually, the process starts with a simple sketch of the satellite, focused on the best location for the payload, ash shown in Figure 4. With a basic configuration, subsystems are integrated to support the payload's power, data handling, communications, attitude control, propulsion, and thermal control requirements. An overview of subsystem development that supports satellite-on-a-chip is presented in the following sections.

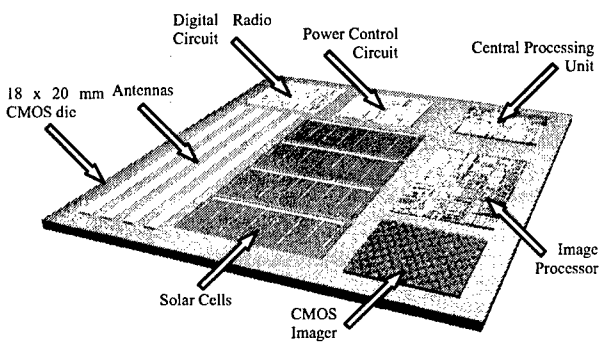

Figure 4. SpaceChip Notional Configuration

As presented in the literature review, there is no unity on the fabrication technique suggested to build a satellite-on-a-chip with three competing methods: miniaturised, MCM, and monolithic. The only publication that has proposed a strictly monolithic approach was written by the author [1]. The final satellite-on-a-chip configuration will be as monolithic as possible, but in summary, a configuration of two CMOS dies back-to-back to meet minimum design requirements will emerge.

To make the idea more concrete, let us assume that a satellite-on-a-chip could be built on a modern semiconductor process available for prototype runs, such as the austriamicrosystems 0.35μ process optimised for integrated CMOS imaging applications. The mass of a typical 200 mm (or 8 in. diameter reference) silicon wafer would have a mass of nearly 55 g, assuming a density of silicon of 2330 kg/m^3 and an average wafer thickness of 0.75 mm. However, the maximum reticle area limits the die mass to 1 g.

SPACECHIP ELECTRICAL POWER SUBSYSTEM

A spacecraft EPS is typically composed of four basic functions: power source, energy storage, power distribution, and power regulation and control [76]. The most important issue to address then is the power source and energy storage, as distribution, power regulation and control have already been addressed in the literature [53].

Typical spacecraft designs can consider using various implementations of solar, chemical, or even nuclear power generation techniques. Chemical and nuclear technologies are not suitable as they go well beyond the confines of the satellite-on-a-chip definition. Solar energy is the option that remains. Because we are unlikely to use some type of thermal conversion technique, the obvious choice is photovoltaic (PV) cells. As discussed in the literature review, the best efficiency achieved for integrated solar cells in CMOS is only 1%.

Now we have enough data to perform a preliminary sizing of the EPS system. Typically, the gross assumption is that 40% of the operating power will come from the payload, which is assumed to be no more than 80 μW from previous work [79]. The total power budget of the payload and all subsystems would then be approximately 200 μW. However, in our design, the communication system, described later in this section, will dominate the power budget, requiring a full milliwatt of electrical power. Using this data and other basic assumptions, Table 3 presents the basic power budget, which comes to a total of 1.13 mW.

Table 3. SpaceChip Power Budget

	Typical	**Design**	
Payload	40.00%	80	μW
EPS	15.00%	30	μW
DH	10.00%	10	μW
Comm	30.00%	**1**	**mW**
ADCS	5.00%	10	μW
Propulsion	0.00%	0	
Thermal	0.00%	0	
Structure	0.00%	0	
	100%	**1.13**	mW

One major design parameter that must be known before EPS sizing can continue is the orbit description. An assumption is made here, simply be based on the fact that any demonstration mission will most likely be hosted by a future SSTL remote sensing satellite, which normally fly in 686 km sun-synchronous orbits. This gives a semi-major axis a of 7064 km, a period P of 98.5 min using Equation 1 and an earth angular radius ρ of

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64.5 degrees using Equation 2, assuming an Earth radius of $R_\oplus$ of 6378 km and a gravitational parameter $\mu_\oplus$ of 3.986x105 km^3/s^2. The time in the eclipse T_e is then found to be 35.7 min using Equation 3, which when taken from the total orbital period, gives a time in the sun T_s of 58.9 min.

$$P = 2\pi\sqrt{\frac{a^3}{\mu_\oplus}} \tag{1}$$

$$\rho = \sin^{-1}\left(\frac{R_\oplus}{R_\oplus + h}\right) \tag{2}$$

$$T_e = \frac{2\rho}{360^\circ}P \tag{3}$$

One other essential decision must be made before proceeding with the EPS sizing. Typically, satellites allocate a portion of the EPS budget to battery charging so that limited operations can continue in the eclipse period of the orbit. If 10% of the EPS budget were used as an estimate for "keep alive power," for example, to keep the volatile memory intact, this would be approximately 100 μW. The power storage required is simply the product of the power needed in the eclipse and the time in the eclipse, which is a requirement of 214 mWs or 214 mJ.

The only way to store energy in CMOS is with an integrated capacitor. This can be done by laying out large planes of metal, separated by an insulating layer of silicon dioxide. Capacitors in CMOS have been commonly used in analogue applications for some time [80]. To calculate the necessary capacitor size to store this energy, we simply use the capacitor energy storage Equation 4, an operating voltage of 2.5V, and the energy result w of 214 mJ found before. This gives a capacitance, C, of 68.5 mF, which is a very large result. A typical capacitance area value for CMOS processes is 4.8 $fF/\mu m^2$. A capacitor the size of the 18 x 20 mm reticle would only produce a capacitance of 1.7 μF, near 40,000 times less than required! With this dismal result, it is apparent that if eclipse operations are desired, a non-monolithic approach must be considered. For the time being, eclipse operations will not be considered.

$$w = \frac{1}{2}Cv^2 \tag{4}$$

To continue the EPS sizing problem, we must now determine the required power output of the solar cells P_{sa} using Equation 5. Assuming a transmission efficiency during the day X_d of 0.85 an eclipse power requirement P_e of zero, the power required out of the solar array is 1.33 mW.

$$P_{sa} = \left(\frac{P_d T_d}{X_d} + \frac{P_e T_e}{X_e}\right)/T_d \tag{5}$$

Finally, we must determine the area of the solar array itself using Equation 6. For now, this calculation will have to make a major assumption about the average incidence angle θ on the satellite. Since we basically have a two-dimensional structure, we lose the advantage of having a more cube-like shape, where at least more than one surface is illuminated at all times. The power output from a solar array is not linear, but instead is a cosine function of the angle of incident light from the normal. However, for the sake of simplicity, we will assume at this time an average θ of 45°. The average annual solar flux value is 1358 W/m^2. As stated previously, the assumed efficiency η is 1%. I_d is assumed to be near 100%, as it represents the inherent degradation of a large solar array constructed of individual solar cells that are soldered together. Although this value is typically 90%, it is assumed to be higher due to the monolithic integration.

With all these preliminary assumptions, we find a beginning-of-life power output P_{BOL} of 9.6 W/m^2. End-of-life power output does not need to be considered for a week-long mission, but is usually 3% per year for silicon based solar cells. This result then gives us an approximate area of only 12x12 mm. This is a promising result, as this is approximately one-third of the reticle, leaving the remaining area for the payload and other systems, which each will be much smaller.

$$P_{BOL} = (solarflux)(\eta)(I_d)\cos\theta \tag{6}$$

A final note on the other basic EPS components responsible for power distribution, regulation, and control. Power distribution is simply the wiring that will be used to provide power to the various systems. Power regulation will ensure that power coming from the source (either solar generated or stored power) will be delivered to the remaining systems at a regulated voltage. We can implement a simple regulation scheme using resistors, diodes, transistors, and capacitors, all which can be built in silicon. Finally, power control can be simply implemented by using basic CMOS switches to switch various components of the subsystems [53].

Another broad-scope issue that complicates the puritan satellite-on-a-chip configuration is that the resulting design is inherently two-dimensional utilizing one side of the wafer. Such a configuration is unacceptable, as the system could go long periods of time without power if the inactive side faces the sun. Due to these physical constraints, a proposed deviation from the pure satellite-on-a-chip definition should be considered. SpaceChip could be composed of two identical 18x20 mm die sandwiched together, with the active sides facing outward. Neither WSI nor die bonding will be used, as only one side at a time will be illuminated.

SPACECHIP DATA HANDLING SUBSYSTEM

The data handling subsystem is basically the on-board computer for the satellite, responsible for several jobs. It receives, validates, decodes, and distributes commands from the ground, payload, or a subsystem to other spacecraft subsystems. It also gathers, processes, and formats spacecraft housekeeping and mission data for

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downlink or use on board. This subsystem is usually the most difficult to define early in the design due to the vague hardware and software requirements from the payload and subsystems.

At a minimum, however, we would expect it to be composed of a central processing unit (CPU) that can understand basic commands and execute them. It will also have various types of volatile memory. A tough part of its design is the interface requirements to the other systems. This usually involves analogue-to-digital converters to measure voltage and temperature [80].

The SpaceChip data handling subsystem will be composed of a small microcontroller that is custom-designed for this application, versus using a power hungry and unnecessarily over-capable CPU core. This microcontroller will be synthesized from hardware description language code that describes the minimum functionality.

To power up and run any CPU, a reset function and external clock are normally required. To provide the reset signal, a simple on-chip pull-up resistor can be used. For our application, a clock source can be generated on chip with a simple ring oscillator. To further enhance the design, asynchronous logic may be explored to eliminate the clock signal and reduce power, which has been investigated previously [81].

Besides taking a RISC microcontroller approach, a top-level design issue that plagues data handling systems operating in space is the natural radiation environment. The radiation environment is composed ionizing radiation that causes gradual system degradation and high-energy particles, such as electrons, protons, and heavy ions, causing single event phenomena. A full description of the damage process in CMOS due to radiation cannot be given here, but its effects are summarised here [82].

In LEO, where we are proposing to fly, the pervasive problem is single event upset. However, total ionizing dose is still an issue for longer missions or applications such as this, where we are essentially flying an unshielded bare die. System engineers typically apply a variety of mitigation strategies against radiation at all levels, starting with the basic shielding of the spacecraft structure itself. However, since we are basically flying a bare silicon wafer with a very thin layer of passivation, a novel approach must be used.

High energy particles in LEO can cause single event effects (SEE), such as upset (SEU), which is temporary, and latchup (SEL), which can only be restored by power cycling and can be permanently damaging in extreme cases. Most space systems using commercial electronics employ error detection and correction (EDAC) techniques utilising multiple redundant systems running in parallel and "vote." This way, if an SEU occurs in one system producing an erroneous result, the majority result allows the process continues without error. This type of EDAC scheme adds complexity, cost, and additional power requirements

The problem can be more elegantly solved at the integrated circuit level using a CMOS device layout technique called "hardened by design" to mitigate both total ionizing dose and single event phenomena as illustrated in Figure 4.

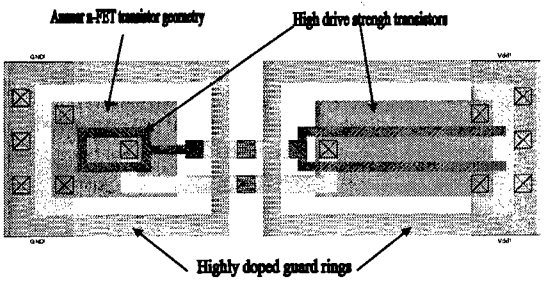

Figure 5. Radiation Hardened By Design Inverter

The technique is not without fault, as there are power and area penalties. By laying out the n-type transistors in an annular shape, the mechanisms that cause transistor leakage from ionizing radiation are eliminated. Increasing the drive strength (length) of the transistors themselves increases the threshold where single event upsets occur from a high-energy particle strike. Finally, adding p+ and n+ (highly doped material normally available in a CMOS fabrication process) guard rings around the transistor areas prevent SEL [82].

SPACECHIP COMMUNICATIONS SUBSYSTEM

An obvious challenge for a satellite-on-a-chip is the communications link between the ground and the satellite. In addition, the satellite-on-a-chip concept presents an additional unique challenge. First, due to its limited size, the onboard RF transmit power must be significant for an effective downlink. Early calculations revealed that the corresponding electrical power to generate the minimum RF power would require an integrated solar array area of at least 50 cm^2, which is well outside of the 3.6 cm^2 area of the largest die.

Another challenge is that the ground station must know exactly where the satellite is to avoid pointing losses with its required high gain antennas. Due to the extremely small size of a satellite-on-a-chip, it is unlikely that current space surveillance networks would be able to detect it and provide orbital element data.

The strategy to meeting these challenges is to avoid them altogether. A possible architecture would rely on a supporting microsatellite in orbit that can serve as a relay to the ground station. Then, numerous satellites-on-a-chip could be evenly distributed in that orbit with a maximum separation of only a few kilometres, using each other as wireless network nodes, ultimately

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communicating with the ground station via the supporting microsatellite. A low-power on-chip digital radio could be implemented for communication over those short distances.

The requirement for the communication subsystem is to communicate between SpaceChips and the on-orbit supporting microsatellite using an integrated digital radio solution. It was initially determined that an RF transmit power of 1 μW could be achieved with an electrical power input of 1 mW, which has been budgeted for in the EPS design. Although coming up with the RF power was easy to solve, other non-trivial design issues that may arise are the integrated antenna design and EDAC, although these have been previously demonstrated in single-chip solutions.

In order to evaluate the communication crosslink, we can solve Frii's transmission Equation 7, for one desired parameter knowing all the others.

$$\frac{E_b}{N_0} = \frac{P_t L_l G_t L_s L_a L_r L_p G_r}{k T_S R} \quad (7)$$

Appropriate worst-case parameters for a notional crosslink are the following: frequency of 2.4 GHz, data rate of 300 bps, range of 1 km, (λ/4) antennas (3.4 cm), and binary phase-shift keying modulation (BPSK) with EDAC. With these parameters, it is possible to achieve a positive comm link margin. However, there is still a fundamental problem here, as (λ/4) antennas cannot be placed on the largest die possible. Unfortunately, the best results in literature show that integrated antennas in CMOS yield a effective communication range of only a few meters [63].

SPACECHIP ATTITUDE AND ORBIT DETERMINATION AND CONTROL SUBSYSTEM

The AOCS system is usually further thought of and divided into the attitude (ADCS) and orbit control (OCS) segments. Spacecraft ADCS keeps it pointing in a desired direction to meet mission requirements, such as to take a picture, keep the solar arrays pointed towards the sun and antennas pointed towards the ground station. A variety of sensors and actuators can accomplish this using active and/or passive means.

To keep the spacecraft pointed in a desired direction to meet mission requirements, the current attitude must be determined with certain accuracy over a given range. Once the current attitude is known, it must be controlled to a specified accuracy, while meeting range, jitter, drift, and settling time requirements. Not only does the satellite and earth motion play a part here, small disturbance torques from the atmosphere, earth's magnetic field, gravity gradient and solar radiation pressure complicate the problem.

In general, satellite designers can meet pointing requirements by using active and/or passive means. The simplest systems with nadir-pointing requirements typically employ a passive gravity gradient boom to achieve crude pointing then fine-tune it with electromagnets (magnetorquers). The magnetorquers must be controlled with an algorithm that has the knowledge of where the spacecraft is pointing, usually by using a sun sensor coupled with compass-like devices (magnetometers). The magnetorquer with magnetometer combination is especially advantageous to small satellites, due to the mass savings [83]. More demanding pointing requirements use a combination of star sensors, differential GPS, or solid-state gyroscopes to determine attitude. The attitude can then be controlled with biased or unbiased reaction wheels, control moment gyros, or thrusters. Thrusters, of course, imply a propulsion subsystem, which is discussed next.

To determine spacecraft attitude, MEMS gyroscopes at first seem to be a likely candidate technology for monolithic integration. At this time, MEMS technology cannot be directly integrated on high-density CMOS. All other sensors currently used in small satellites are still major sub-components, many times the size of a CMOS chip. So, it is apparent, that attitude determination will not be able to be accomplished.

Fortunately, the omnidirectional communications antennas do not impose a pointing requirement. The only real practical consideration is to keep the body rates down enough where one side of SpaceChip could face the sun for a long enough time to take a picture and transmit the data. Granted, on any given attempt, SpaceChip may not be pointing at the Earth. Hopefully, over the course of several attempts, an image or partial image could be captured.

In order to stabilise the attitude on this simple mission, we can use two methods of passive control. First, we will simply implement an inductor on chip [87] to act as a passive magnetorquer in the x-axis, which is in the plane of the die. This will cause the x-axis to line up with the earth's magnetic field lines, which run roughly north to south. With the single magnetorquer, the y-axis, which is also in the plan of the die, and the z-axis, which is orthogonal to the die, to freely rotate about the x-axis. The detailed design investigates the number of turns of "wire" that could be placed on the wafer, the current required, and the torque produced. A trade-off would then be found based on the torque required and the available electrical power.

The second method of attitude control is passive aerodynamics. A "drag tail" will be employed on one edge to give that part slightly more drag. Hopefully this will keep SpaceChip from spinning around the x-axis stabilized by magnetic force. A similar nanosatellite application has been proposed [85].

The OCS is a problem of navigation, guidance, and control (NGC). Ideally, once a satellite is placed in the

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desired mission orbit by the launch vehicle, it will stay there forever. However, there are many external forces that cause the simplified earth-satellite two-body system to behave in a non-idealistic fashion. The first contributing factor is the oblateness (i.e. it is not a perfect sphere) of the earth that affects all orbits. The second factor is the drag environment that is significant in orbits less than 1000 km in altitude.

Accelerometers and gyroscopes have typically accomplished the precision navigation function, augmented by periodic position information uploaded from space surveillance networks. MEMS accelerometers are also available, but again, cannot monolithically integrate in CMOS. Recently, GPS has been acknowledged as an independent and reliable method for determining spacecraft position and velocity for small satellites. A version for a nanosatellite has already been demonstrated [84]. Single-chip solutions have been demonstrated as well [88]. However, even the smallest commercial product on the market now relies on dual-chip solutions with numerous external passive components to realise a 16x19x3 mm package and uses 30 mW of power.

To complete the NGC picture, a propulsion subsystem is needed to adjust the orbit to the desired state. To complete the spacecraft subsystem survey, the next section addresses the possibility of integrating a propulsion subsystem.

SPACECHIP PROPULSION SUBSYSTEM

Surprisingly, a fair amount of work has been focused on propulsion for very small satellites. These efforts are generally divided up into three categories: non-propulsive, miniaturised, and digital. A novel non-propulsive method has been proposed for picosatellites where a deployable wing is used in LEO to adjust various orbital elements except altitude boosting [86]. There is other promising research in miniaturizing the components of existing thruster concepts, but none of them can be integrated into CMOS.

The most promising technology that is applicable to satellite-on-a-chip is the digital micro-propulsion effort [89]. This technology embeds discreet amounts of propellant in an array of sealed capsules on a silicon substrate. When the appropriate control lines are activated, then the propellant is heated and released. However, at present, this technology requires very high activation voltages, is difficult to deliver symmetric thrust, and cannot be integrated in CMOS.

SPACECHIP THERMAL SUBSYSTEM

There are no significant works, nor are they needed, on small spacecraft thermal control. Early calculations reveal that the expected steady-state hot and cold temperatures expected are slightly out of the desired range. Any thermal issues encountered will be handled using passive methods, such as phase changing materials.

Thermal control is an important issue, even for something as small as a satellite-on-a-chip. This first order design simply looks at the steady-state maximum and minimum temperatures that the spacecraft would encounter. These two points will simply serve as bounds to the problem, knowing that dynamic sunlight-eclipse cycles will not allow time for extremes to be met.

Using the solar array modelling process in SMAD, we can reasonably calculate the temperature extremes a satellite-on-a-chip can experience, worst case. The solar absorptivity constant α for a silicon wafer is 0.48 and the infrared emissivity ε is 0.46 [90]. Using the previous value of ρ from Equation 2, we find the view factor of a flat plate normal to a sphere (the Earth) F_p to be 0.86 using Equation 8.

$$F_P = \sin^2 \rho \tag{8}$$

K_a then compensates for collimated sunlight reflecting off the earth then hitting the flat plate, which is found to be 0.996 using Equation 9.

$$K_a = 0.664 + 0.521\rho - 0.203\rho^2 \tag{9}$$

Then, assuming the standard hot case values solar flux at earth G_s of 1418 W/m^2, percentage of reflected light from sun off earth, or albedo a of 35%, earth infrared value q_I of 258 W/m^2, and the Stefan-Boltzmann's constant σ, we find the maximum temperature to be 96°C using Equation 10.

$$T_{\max(SA)} = \left[\frac{\alpha_t G_S + \varepsilon_b q_I F_P + \alpha_b a G_S K_a F_P - G_S \eta}{\sigma(\varepsilon_b + \varepsilon_t)} \right]^{1/4} \tag{10}$$

Using the standard cold case earth infrared value of q_I of 216 W/m^2, the minimum temperature is found to be –74°C using Equation 11.

$$T_{\min(SA)} = \left[\frac{\varepsilon_b q_I F_P}{\sigma(\varepsilon_b + \varepsilon_t)} \right]^{1/4} \tag{11}$$

This temperature range is concerning, as they indicate a large swing in temperatures during an orbit. In addition, the temperatures are out of the range of most battery technologies (0 to +25°C) and industrial grade electronics (-40 to +85°C). These results would have to be verified in the laboratory and possibly solved by using a simple phase-changing thermal management substrate such as paraffin that the wafers would be adhered to in order to narrow the temperature range.

CONCLUSION

The concept of satellite-on-a-chip has been assessed by the notional design of SpaceChip. While much of the design is a straightforward application of current technology, there are several critically limiting issues. The single most limiting technology is the area of on-chip integrated antennas for communication over the air. The best results to date have only achieved a maximum of 5

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meters. With this short range, a very dense cluster of SpaceChips would have to exist for any communication to occur between nodes.

The next issue that limits application of SpaceChip is the native problem of low efficiency solar cells on commercial CMOS. To date, only 1% efficiency has been achieved. Even so, this assumption was taken into account, giving an adequate power budget of 1 mW

The third critical limiting technology is integrated orbit and time determination and orbit control. To perform any meaningful science mission, the time and location where a measurement was taken would be essential. For control, no current propulsion options exist, limiting its application.

Finally, on-chip sensor technology in CMOS is fairly limited. Additional sensor technologies would have to be researched and developed in order to SpaceChip as a viable technology. The remaining issues such as attitude and thermal control, while challenging, can be solved with a modest engineering effort.

To complete the satellite-on-a-chip feasibility assessment, a risk assessment is presented, highlighting the greatest challenges ahead. Table 4 outlines the required technology areas and identifies the risk associated with developing and integrating each particular technology.

Table 4. SpaceChip Risk Assessment

Technology Area	Low	Medium	High	Exclude
Satellite-on-a-chip		✓		
CMOS imager payload	✓			
Integrated photovoltaic cells			✓	
Data handling system-on-a-chip	✓			
Digital radio system-on-a-chip			✓	
Femtosatellite attitude control		✓		
Thermal control	✓			
Propulsion system-on-a-chip			✓	✓
Integrated MEMS and GPS			✓	✓

Overall, the satellite-on-a-chip concept is considered medium risk. It is certainly feasible to create a solar-powered intelligent CMOS imager. The integrated radio component will be a challenge but should be feasible with limited application. Incorporating ionising radiation mitigation, attitude and thermal controls will be the icing on the cake that makes the design suitable for space applications. The design itself will contribute to the field of distributed missions, but certainly that problem is far from being solved and will require much more research and development before it is widely used.

The first SpaceChip mission concept and spacecraft design has been presented. A simple low-resolution Earth imaging mission has been proposed. The resulting design will be a near satellite-on-a-chip implementation, with adaptations for an external lens and two-sided configuration for power and thermal control requirements. An outline of the basic specifications is presented in Table 4.

Table 5. SpaceChip System Specifications

Mission	Simple low-resolution Earth observation mission, image taken within a week of separation
Orbit	Sun-synchronous 686 km/98 deg
Configuration	Two-sided spacecraft composed of a thermal substrate sandwiched between two CMOS die
Dimensions	18 x 20 x 3 mm
Mass	~10 g
Payload	4K pixel CMOS imager with integrated microlenses
EPS Budget	~1 mW
Data Handling	On board storage of one image, device layout level single event upset mitigation strategy
Communications	Digital transceiver with 1 μW RF output (~5 m range)
Attitude Determination and Control	Passive magnetic and aerodynamic stabilization
Orbit Control/Propulsion	None for first mission
Thermal Control	Passive substrate

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